METHOD FOR MANUFACTURING INTERLAYER DIELECTRIC LAYER IN A SEMICONDUCTOR DEVICE

Field of the Invention

The present invention relates to a semiconductor device; and, more particularly, to method for manufacturing an interlayer dielectric (ILD) layer with an enhanced gap-fill capability using a tetra-ethyl-ortho-silicate (TEOS) and a hydrogen peroxide (H_2O_2) as a source material.

Description of the Prior Art

As is well known, a semiconductor memory device has a higher degree of integration mainly by down-sizing through micronization. However, there is still a demand for downsizing the area of the memory cell.

To meet the demand, therefore, there have been proposed several methods, such as a trench type or a stack type capacitor, which is arranged three-dimensionally in a memory device to reduce the cell area available to the capacitor.

In employment of this structure of a capacitor, however, a high topological difference is produced between a memory cell region and a peripheral circuit region. Thus, the three-dimensional structure for the high degree of the integration causes a bad gap-fill capability and a step coverage when forming various layers, e.g., interlayer dielectric (ILD)

layer, on a semiconductor substrate. Therefore, in a deposition of the interlayer dielectric layer, there are problems of the bad gap-fill capability and the step coverage, whereby a void may exist in the interlayer dielectric layer after the deposition.

Referring Figs. 1A to 1E, there are shown cross sectional views setting forth a conventional method for manufacturing a semiconductor device incorporated therein the ILD layer.

The manufacturing steps begin with a preparation of a semiconductor device 110 of which predetermined manufacturing steps has been carried out in advance. And then, conductive layers are formed on the semiconductor substrate 110 and patterned into a first predetermined configuration, thereby forming interconnections 120. Thereafter, an ILD layer 130 is formed on entire surface, wherein a thickness of the interlayer dielectric layer 130 is higher than heights of the interconnections 120 as shown in Fig. 1A. Here, a distance between each interconnection 120 is narrow and the height of the interconnections 120 is high so that an aspect ratio increases. Thus, a gap-fill capability is deteriorated in depositing the ILD layer 130 so that there is a void 115 remaining in the ILD layer 130.

The conventional method for forming the ILD layer 130 is illustrated in more detail hereunder.

To begin with, after reacting tetra-ethyl-ortho-silicate (TEOS) with active oxygen such as O_3, O_2 and N_2O, the TEOS and the active oxygen are deposited on the substrate 110, thereby

forming the ILD layer 130. Thereafter, the ILD layer 130 is annealed above 800 ℃ for densification.

In a next step as shown in Fig. 1B, a top surface of the ILD layer 130 is flattened by using a chemical mechanical polishing (CMP) process, wherein a flattened top surface of the ILD layer 130 is also higher than those of the interconnections 120. Subsequently, a photoresist layer 140 is formed on the flattened top surface of the ILD layer 130.

In an ensuing step as shown in Fig. 1C, the photoresist layer 140 is patterned into a second predetermined configuration by using a method such as a photolithography, thereby obtaining photoresist patterns 140A.

In a subsequent step, the interlayer dielectric layer 130 is patterned into the second predetermined configuration using the photoresist pattern 140A as a mask, thereby obtaining a contact hole 135. Here, while patterning the ILD layer 120 by an etching step, a polymer is accumulated in the void 115 so that the polymer in the void 115 plays a role as an etching barrier, whereby a residue 125 of an oxide remains between the void 115 and the semiconductor substrate 110 as shown in Fig. 1D.

Finally, the photoresist patterns 140A are stripped off so that whole the manufacturing steps are completed as shown in Fig. 1E, wherein the residue 125 of the oxide remains still on the substrate 110.

In the conventional method for forming the ILD layer, there may be a void therein so that the residue 125 of the

oxide may remain after the etching step. Thus, the residue 125 causes the device to fail eventually. Furthermore, since the annealing process for densification is carried out at a high temperature, i.e., above 800 ℃, the other layers such as a metal silicide, silicide, a metal nitride, or the like, is deteriorated during the annealing process. To overcome this problem, another method for forming the ILD layer using SiH_4 and H_2O_2 is developed. However, this method also has a problem of bad reproducibility because it is carried out at approximately 0 ℃. In addition, it may cause a crack due to an unstable deposition layer after the annealing process.

Summary of the Invention

It is, therefore, an object of the present invention to provide method for manufacturing an interlayer dielectric (ILD) layer with a good gap-fill capability by using a tetra-ethyl-ortho-silicate (TEOS) or modified TEOS and H_2O_2 as a source material.

In accordance with one aspect of the present invention, there is provided a method for manufacturing an interlayer dielectric layer, the method comprising the steps of: a) setting an active matrix provided with a substrate and interconnections formed on the substrate in a chamber; b) spraying a silicon source material and a hydrogen peroxide (H_2O_2) in a gaseous state on the active matrix; and c) forming the interlayer dielectric layer on the active matrix by a

condensation reaction of the silicon source material and the H_2O_2.

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

Figs. 1A, 1B, 1C, 1D and 1E are schematic cross sectional views setting forth a conventional method for manufacturing a semiconductor device incorporated therein an interlayer dielectric (ILD) layer;

Figs. 2A, 2B, 2C, 2D and 2E are schematic cross sectional views setting forth a method for manufacturing a semiconductor device incorporated therein an interlayer dielectric (ILD) layer in accordance with a preferred embodiment of the present invention; and

Fig. 3 is a schematic view of an apparatus for forming an ILD layer.

Detailed Description of the Preferred Embodiments

There are provided in Figs. 2A to 2E cross sectional views setting forth a method for manufacturing a semiconductor device incorporated therein an interlayer dielectric layer (ILD) in accordance with a preferred embodiment of the present

invention.

The manufacturing steps begin with a preparation of a semiconductor device 210 of which predetermined manufacturing steps has been carried out in advance. And then, conductive layers are formed on the semiconductor substrate 210 and patterned into a first predetermined configuration, thereby forming interconnections 220. Thereafter, an ILD layer 230 is formed on entire surface using a tetra-ethyl-ortho-silicate (TEOS) and a hydrogen peroxide (H_2O_2) as a source material, wherein a thickness of the ILD layer 230 is higher than heights of the interconnections 220.

The process for forming the ILD layer 230 is illustrated in more detail hereunder.

Referring to Fig. 3, there is provided a schematic view of an apparatus for forming the ILD layer 230. To begin with, a wafer 312 is set on a susceptor 314 in a chamber 310, wherein a temperature controller 316 is attached to the susceptor 314 for modulating a deposition temperature. Thereafter, a source material, e.g., TEOS and H_2O_2, is supplied into the chamber 310 through a each flow rate controller (F/C) 320, 324, wherein the TEOS and H_2O_2 are maintained in liquid state by employing a method such as a ultrasonic spray, vacuum vaporization or the like. Subsequently, the TEOS and H_2O_2 are deposited on the wafer 312 through a distributor 318. When the TEOS and H_2O2 are supplied into the flow rate controllers 320, 324, inert gas, e.g., Ar, He, Ne or the like, is supplied from supplying

devices 322, 326 simultaneously. Meanwhile, when the TEOS and the H_2O_2 in a gaseous state are supplied into the chamber 310, inert gas is supplied simultaneously from an auxiliary supplying device 328 to enhance uniformity in the chamber 310. It is preferable that the temperature and the pressure in the chamber range from approximately -20 ℃ to approximately 600 ℃ and approximately 1 Torr to approximately 2 Torr, respectively.

Referring back to Fig. 2B, there is shown a state after a deposition step progresses for a predetermined time. In this figure, the ILD layer 230 is successfully formed between the interconnections 220 without a void. In more detail, the TEOS and H_2O_2 in the gaseous state, which are supplied into the chamber 310 through the distributor 318, react with each other on a surface of the wafer 310. Therefore, a chemical structure of the TEOS, i.e., (C_2H_5O)-Si-(OH_5C_2), is changed into (C_2H_5O)-Si-O by means of active oxygen ions separated from the H_2O_2. Especially, Si-O bond or Si-OH bond produced from the above reaction, has a characteristic that they are easily bonded with each other so that -O-Si-O- bond is formed by a condensation reaction. From the condensation reaction, by-product of H_2O plays an important role in inhibiting the violent reaction with the TEOS and the H_2O_2. And further, an intermediate material 240 such as (C_2H_5O)-Si-O and (C_2H_5O)-Si-OH, has a high fluidity, thereby obtaining a good gap-fill capability.

In a next step as shown in Fig. 2C, a top surface of the

ILD layer 230 is flattened by using a chemical mechanical polishing (CMP) process, wherein a flattened top surface of the ILD layer 230 is also higher than those of the interconnections 220.

In an ensuing step as shown in Fig. 2D, a photoresist layer is formed on the flattened top surface of the interlayer dielectric layer 230 and patterned into a second predetermined configuration by using a method such as a photolithography, thereby obtaining photoresist patterns 250.

In a subsequent step, the ILD layer 230 is patterned into the second predetermined configuration using the photoresist pattern 250 as a mask, thereby obtaining a contact hole 260. Here, in patterning the ILD layer 230 by an etching step, there is not any etching barrier in comparison with a prior art. Finally, the photoresist patterns 250 are stripped off so that whole the manufacturing steps are completed as shown in Fig. 2E.

In the present invention, the TEOS and the H_2O_2 are used for depositing the ILD layer, but it is possible to add an impurity material such as boron (B), phosphor (P), B and P or the like, to the source material of the TEOS and the H_2O_2. That is, in case of using TEB, TMB or TEB/TMB as a boron dopant, phosphor dopant or B/P-dopant respectively, the ILD layer becomes BSG, PSG or BPSG, respectively.

Moreover, the TEOS may be substituted by a modified TEOS which one of four C_2H_5OH groups in the TEOS is substituted by a group of CH_3 or F. In case of using the modified TEOS

instead of the TEOS, the interlayer dielectric layer becomes a low dielectric silicon oxide like ($SiOx(CH_3)y$) or (SiO_xF_y).

In comparison with the prior art, the present invention provides a method for manufacturing the ILD layer with a good gap-fill capability. Additionally, the present invention has an advantage that the ILD layer can be formed without a post thermal treatment at above 800 ℃.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.